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PTO/SB/08A (08-00)

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Substitute for Form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete If Known	
			Application Number	09/992,387
			Filing Date	11/16/01
			First Named Inventor	Anthony L. Coyle
			Group Art Unit	2822
			Examiner Name	Lewis, M.
Sheet 1 of 1	Attorney Docket No.	TI-31794		

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
mc	AA	6,166,433		Takashima et al.	12/26/00	
mc	AB	6,157,084		Hino et al.	12/05/00	
mc	AC	5,814,894		Igarashi et al.	09/29/98	
	AD					
	AE					
	AF					
	AG					
	AH					

FOREIGN PATENT DOCUMENTS

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		Office ³	Number ⁴	Kind Code ² (if known)				
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	CA		
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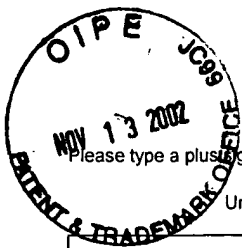
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(use as many sheets as necessary)				Attorney Docket No.	TI-31794
Sheet	2	Of	2		

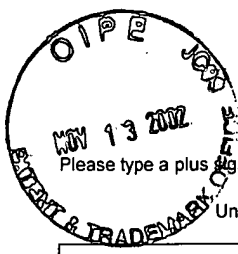
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MC	CA	"Controlled Collapse Reflow Chip Joining", L.F. Miller, IBM J. Res. Develop., IBM Components Division, Vol. 13, 1969, pp. 239-250	
	CB	"Geometric Optimization of Controlled Collapse Interconnections", L.S. Goldman, IBM J. Res. Develop., Vol. 13, 1969, pp. 251-265	
	CC	"Parametric Study of Temperature Profiles in Chips Joined by Controlled Collapse Techniques", S. Oktay, IBM J. Res. Develop., IBM Components Div., Vol. 13, 1969, pp. 272-285	
	CD	"Reliability of Controlled Collapse Interconnections", K. C. Norris and A. H. Landzberg, IBM J. Res. Develop., IBM Components Division, Vol. 13, 1969, pp. 266-271	
	CE	"SLT Device Metallurgy and Its Monolithic Extension", P.A. Totta and R. P. Sopher, IBM J. Res. Develop., IBM Components Division, Vol. 13, 1969, pp. 226-238	
MC	CF	"Studies of the SLT Chip Terminal Metallurgy", B.S. Berry and I. Ames, IBM J. Res. Develop., Vol. 13, 1969, pp. 286-296	
	CG		
	CH		
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	CM		
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	CQ		
	CR		

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M	AA	5,928,458		Aschenbrenner, et al.	07/27/1999	
	AB					
	AC					
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